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Design, Simulation & Optimization of 45nm NMOS Transistor

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Abstract: This paper focuses on the result of process & device simulation using SILVACO TCAD tools to develop and optimize 45nm NMOS electrical characteristics using Gaussian doping profile. Fabrication process of transistor was performed in Athena while electrical characterisation of device was performed by ATLAS simulator. The analysis focussed on I_D-V_{GS} curve, I_G-V_{DS} curve, threshold voltage, ON and OFF currents, DIBL estimation, dependency of threshold voltage on various parameters like gate oxide thickness, V_{TH} adjust implant doping concentration and Halo implant doping concentration . From the simulation result, optimum solution of threshold voltage of 0.095V has been achieved.

Index Terms: MOSFET, Silvaco, threshold voltage, DIBL, Athena.

1. INTRODUCTION

The exponentially decreasing size of transistor results in incorporation of large number of transistors on a chip. This fast scaling of MOSFETs results in increased microprocessor performance and rapid growth of information technology revolution.

With the technological evolution and the continuous device miniaturization, several undesirable effects also have appeared for the new technologies. The gate oxide thickness (tox) reduction and the associated increase in the electric field applied across the gate oxide lead to an increase of the transistors's gate leakage current. As the technology scaling is entering the nano meter regime, the dominant problem which come into the scenario are, the increased short-channel effects (SCEs) [1]. Although, the short channel behaviour can be observed experimentally, understanding the limits to scaling and how they relate to different device parameters is very important for the design of next generation MOSFETs.

An important value which characterizes the MOSFET transistors is the value of threshold voltage. The value of the gate-to-source voltage V_{GS} needed to create (induced) the conducting channel (to cause surface inversion) is called the threshold voltage and denoted with V_{TH}. This value can be controlled during the fabrication process of MOSFET transistors. The value of the threshold voltage is dependent on some physical parameters which characterize the MOSFET structure such as: the gate material, the thickness of oxide layer tox, substrate doping concentrations (density) N_A, oxide –interface fixed charge concentrations (density) N_{OX}, channel length L, channel width W and the bias voltage V_{SB}.

The impact of Gaussian profile has been observed on device performance. The leakage current in the device has been calculated. The various process parameters have been calculated e.g threshold voltage, Ion, Ioff, Ion/Ioff ratio and DIBL. The whole work is carried out using Silvaco TCAD tool.

2. DESIGN & SIMULATION

Simulations are performed with a two-dimensional (2-D) device simulator, SILVACO. The physical structure of the scaled MOSFET used in our present study are designed using ATHENA considering the standard Silicon integrated chip processing technology and the electrical characteristics are simulated using ATLAS . A 45nm MOSFET is designed using the following process flow:

Table 1: Specifications to design 45nm NMOS

PROCESS	NMOS DEVICE
Initial substrate doping	Boron=$1.5x10^{15}$ cm^3, Orientation=<100>
p-well implant	Boron=$1.0x10^{12}$ cm^{-2}, Energy=100 KeV
Gate oxide growth	1.0 nm
Vt implant	$1.0x10^{13}$, Energy=1 KeV
Polysilicon thickness	80nm
LDD implant	Arsenic=$1.2x10^{15}$, Energy=1 KeV
Pocket implant	Boron=$5x10^{13}$ cm^{-2}, Energy=25 KeV
Source Drain implant	Arsenic=$3.2x10^{15}$ cm^{-2}, Energy=7.5 KeV
Final Rapid Thermal (RTA)	800°C/1 sec

The physical structure of 45nm NMOS device is designed using ATHENA and the electrical characteristics are simulated using ATLAS device simulator. The specifications of the silicon substrate considered for the design are p-type Boron doped substrate with doping concentration of $1.5x10^{15}$ atoms cm^{-3} and <100> orientation. The design structure consists of SiO_2 dielectric of thickness 1 nm with Polysilicon gate.

3. SIMULATION RESULTS OF 45NM NMOS

The simulation of the MOSFET was done with ATHENA. It is the SILVACO process simulator used for device

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fabrication. ATHENA is always the desired simulator for complex designs realized from true industrial fabrication methods because a structure is developed that is closer to the actual real life device. ATLAS and DEVEDIT extremely simplify the device to a more basic level. ATHENA incorporates each fabrication process into a single framework.

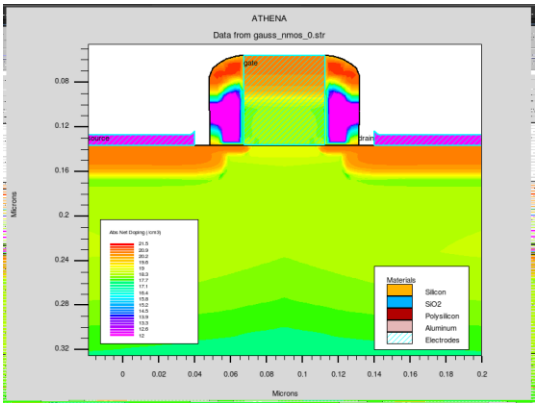

Figure: 1 Athena structure of 45nm NMOS

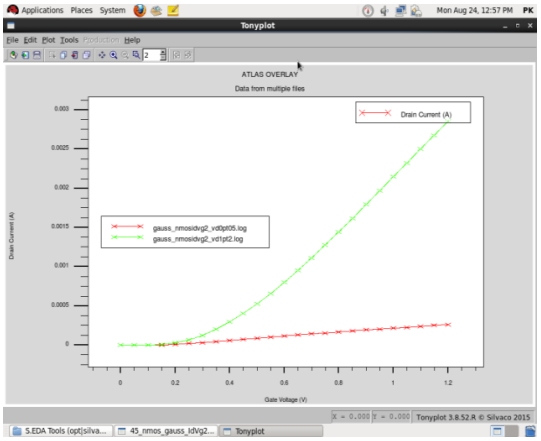

Figure: 2 I_D-V_{GS} curve at different drain voltages

The I_D-V_{GS} characteristics has been observed at different drain voltages at $V_{DS=}$ 0.05V and $V_{DS=}$ 1.2V.

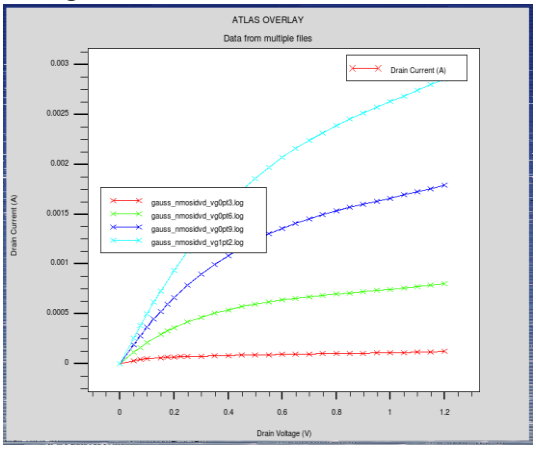

Figure: 3 I_D-V_{DS} curve at various gate voltages

The I_D-V_{DS} characteristics have been observed at various gate voltages. It has been observed that the drain current increases with the increase of gate voltage. After the execution, various parameters has been extracted. These are given below:

Table 2: Extracted Results after Simulation

PARAMETERS	NMOS GAUSS
Gate oxide thickness, tox	1 nm
Threshold Voltage,Vtsat	0.095V
Ion	2854.83 µA
Ioff	0.1176 nA
Ion/Ioff	24269.4
DIBL	0.0374

4. RESULTS AND DISCUSSIONS

4.1 Effect of Oxide Thickness

In a given technology, the threshold voltage depends on the choice of oxide and on oxide thickness. Using the body formula

$$V_T = V_{TO} + \gamma\left(\left(\sqrt{|V_{SB} + 2\phi_F|}\right) - \sqrt{|2\phi_F|}\right) \text{-(1)}$$

where V_{TO} is the threshold voltage when substrate bias is present,[2] V_{SB} is the source-to-body substrate bias, $2\varphi_F$ is the surface potential, and V_{TO} is threshold voltage for zero substrate bias, $\gamma = (t_{ox}/\varepsilon_{ox})\ (2q\varepsilon_{si}\ N_A)^{1/2}$ is the body effect parameter, t_{OX} is the gate oxide thickness, ε_{OX} is oxide permittivity, ε_{si} is the permittivity of silicon, N_A is a doping concentration, q is the charge of an electron., V_T is directly proportional to γ, and t_{OX}, which is the parameter for oxide thickness. Thus, thinner is the oxide thickness, the lower the threshold voltage.

Although this may seem to be an improvement, it is not without cost; because the thinner the oxide thickness, the higher the subthreshold leakage current through the device will be. Before scaling the design features, a dual-oxide approach for creating the oxide thickness was a common solution to this issue. [3].

Table: 3 Gate oxide thickness variations

Gate oxide thickness	Threshold voltage(V)
0.001 µm	0.095
0.0015 µm	0.280
0.002 µm	0.451

The oxidation time, temperature and pressure are the parameters that effect threshold voltage. In this simulation the oxidation time and temperature was modified to get the oxide thickness value in line with ITRS guideline for 45nm device. The corresponding results are given below:

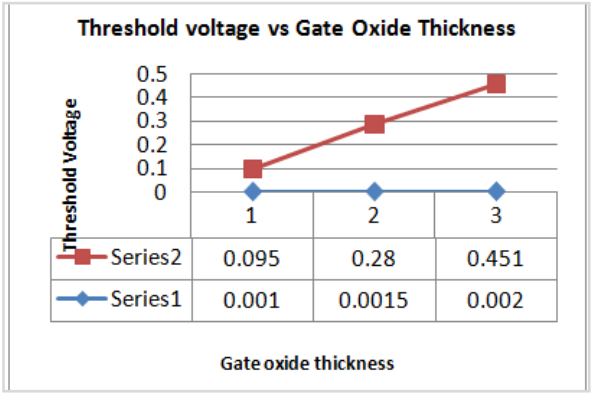

Figure: 4 Threshold voltages at different gate oxide thickness.

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4.2 Effect of V_{TH} adjust implant doping concentration

The most valuable tool for controlling threshold voltage is ion implantation. Since very precise quantities of impurity can be introduced by this method,[4] it is possible to maintain close control of V_{TH}.

The implantation is performed with Boron with an energy of 1 kev and a dose of 1e13 cm^{-2}.The threshold voltage adjust implantation alters the doping profile near the surface of silicon substrate.

Now as we know the threshold voltage is gate voltage above which the transistor becomes conductive due to an inversion of a thin layer below the gate. This voltage which is necessary to create an inversion layer strongly depends on the original doping concentration, which is adjusted by this implantation.

A higher dosage of implant will lead to a higher V_{TH} value because the p channel will be harder to invert for this NMOS transistor.

Table: 4 Vt adjust implant variation

Boron concentration	Threshold voltage
1.0E+13	0.095
1.6E+13	0.228
2.3E+13	0.356

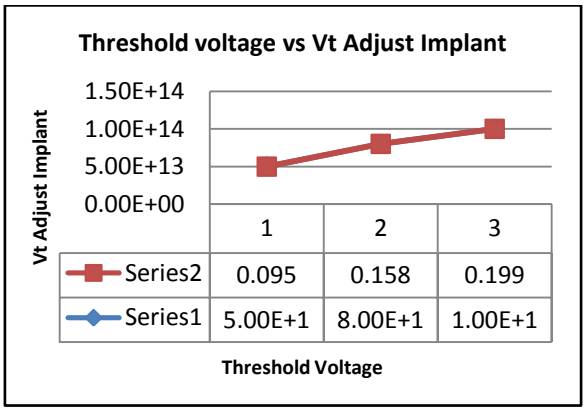

Figure: 5 Variation of threshold voltage at different Vt adjust implantation

So V_{TH} increases when V_{TH} adjust implantation doping increase. Threshold voltage adjust implantations are always performed with low doses, because just slight modification of the gate concentration are sufficient for the adjustment.[5]

4.3 Effect of Halo Implant doping concentration

Halo Implantation is introduced to eliminate the effects of Vth roll-off and short channel effects. It has been observed that with the increase of Halo implant doping concentration, threshold voltage increases.

Table:5 Halo Implant Variation

Halo implant	Threshold voltage
5.0E+13	0.095
8.0E+13	0.158
1.0E+14	0.199

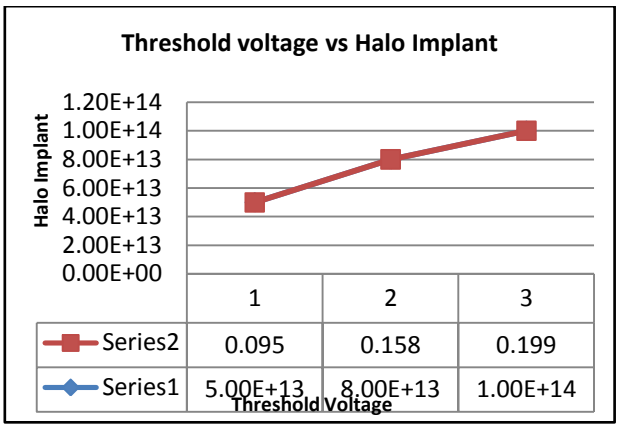

Figure 6: Variation of threshold voltage at different Halo implant concentrations

5. CONCLUSION

The design, simulation of NMOS transistor has been done using Gaussian profile.There are three factors that affect threshold voltage which is channel doping, gate oxide thickness and Halo implantation. V_{TH} value of 0.095V is achieved from this simulation. For 45 nm NMOS, the value is in line with international technology roadmap for semiconductor (ITRS) guideline.

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